Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-20 (canceled)

Claim 21 (currently amended): An integrated circuit comprising:

a first processor unit of the integrated circuit to receive a first clock to control performance of the first processor unit;

a first buffer coupled to receive data from an output of the first processor unit, the first buffer clocked by a master clock;

a second processor unit of the integrated circuit coupled to receive the data from the first buffer and to receive a second clock to control performance of the second processor unit; and

at least one clock controller to generate the first clock and the second clock from the master clock, and to vary a frequency of the first clock and the second clock.

Claim 22 (currently amended): The integrated circuit of claim 21, further comprising a memory of the integrated circuit coupled to the first processor unit and the second processor unit.

Claim 23 (currently amended): The integrated circuit of claim [[21]] 22, further comprising a wireless transceiver coupled to the first processor unit and the second processor unit.

Claim 24 (currently amended): The integrated circuit of claim 21, ~~wherein~~ further comprising a reconfigurable processor core including the first processor unit and the second processor unit ~~comprise a reconfigurable processor core~~.

Claim 25 (previously presented): The integrated circuit of claim 21, wherein the first buffer to provide a feedback signal to the at least one clock controller, the at least one clock controller to vary the first clock based on the feedback signal.

Claim 26 (previously presented): The integrated circuit of claim 21, wherein the first clock is different than the master clock.

Claim 27 (previously presented): The integrated circuit of claim 21, wherein the first processor unit comprises a reduced instruction set computer (RISC) processor.

Claims 28-29 (cancel)

Claim 30 (currently amended): A system comprising:

a first processor to receive a first clock signal to control performance of the first processor;

a first buffer coupled to an output of the first processor, the first buffer coupled to receive the first clock signal; and

a first controller to generate the first clock signal from a master clock, the first controller to receive a first feedback signal from the first buffer and to control the first clock signal based on the first feedback signal ~~to optimize processing power of the first processor~~.

Claim 31 (previously presented): The system of claim 30, further comprising a second processor coupled to an output of the first buffer to receive a second clock signal to control performance of the second processor.

Claim 32 (currently amended): The system of claim 30, wherein the first controller to provide a write signal to the first buffer based on the first feedback signal, wherein the write signal corresponds to the first clock signal.

Claim 33 (previously presented): The system of claim 30, wherein the first controller to lower a frequency of the first clock signal if the first feedback signal is above a threshold.

Claim 34 (previously presented): The system of claim 30, wherein the system comprises a wireless device.

Claim 35 (previously presented): The system of claim 34, further comprising an input sensor coupled to the first processor to receive visual information.

Claim 36 (currently amended): A method comprising:

clocking a first processor of an integrated circuit with a first clock;

clocking a second processor of the integrated circuit with a second clock;

clocking a buffer coupled to provide data from ~~between~~ the first processor ~~and~~ to the second processor with a master clock; and

~~controlling~~ generating a frequency of the first clock and the second clock from the master clock to control performance of the first processor and the second processor.

Claim 37 (cancel)

Claim 38 (previously presented): The method of claim 36, further comprising generating the first clock and the second clock using a controller on a single substrate with the first processor and the second processor.

Claim 39 (currently amended): The method of claim 38, further comprising generating a clock from the master clock to control a wireless transceiver on the single substrate using the controller.

Claim 40 (new): The system of claim 31, further comprising a second buffer coupled to an input of the first processor, the second buffer controlled by the first clock signal.

Claim 41 (new): The system of claim 33, wherein the threshold is adjustable.

Claim 42 (new): The method of claim 36, further comprising maintaining the master clock at a fixed frequency.